Analytical modelling and performance analysis of double-gate MOSFET-based circuit including ballistic/quasi-ballistic effects

S. Martinie[ab]; D. Munteanu[b]; G. Le Carval[a]; J. L. Autran[bc]

[a] CEA-LETI Minatec, Grenoble, France [b] IM2NP-CNRS, UMR CNRS 6242, Marseille Cedex 13, France [c] University Institute of France (IUF), Paris, France

PLEASE SCROLL DOWN FOR ARTICLE

Analytical modelling and performance analysis of double-gate MOSFET-based circuit including ballistic/quasi-ballistic effects

S. Martinie[ab]*, D. Munteanu[b], G. Le Carval[a] and J.L. Autran[bc]

[a]CEA-LETI Minatec, 17 rue des Martyrs, 38054 Grenoble, Cedex 9, France; [b]IM2NP-CNRS, UMR CNRS 6242, Bât. IRPHE, 49 rue Joliot Curie, BP 146, 13384 Marseille Cedex 13, France; [c]University Institute of France (IUF), 75000, Paris, France

In this paper, we present a compact model of double-gate MOSFET architecture including ballistic and quasi-ballistic transport down to 20 nm channel length. In addition, this original model takes into account short-channel effects (SCE/DIBL) by a simple analytical approach. The quasi-ballistic transport description is based on Lundstrom's backscattering coefficient given by the so-called flux method. We also include an original description of scattering of processes by introducing the 'dynamical mean free path' formalism. Moreover, we implemented our model in a Verilog-A environment, and applied it to the simulation of circuit elements such as CMOS inverters and ring oscillators to analyse the impact of ballistic/quasi-ballistic transport on circuit performances. Finally, in order to validate our work, we confronted this model with numerical simulation of CMOS and ring oscillator in ballistic case.

Keywords: double-gate MOSFET; ballistic/quasi-ballistic transport; compact model; ring oscillator

1. Introduction

As the MOSFET continues to shrink rapidly, emerging physical phenomena, such as ballistic transport, have to be considered in the modelling and simulation of ultra-scaled devices. Future double-gate MOSFETs (DGMOS; Figure 1), designed with channel lengths in the decananometre scale, are expected to be more ballistic or quasi-ballistic than diffusive. At this level of miniaturisation is essential to directly evaluate the impact of ballistic and quasi-ballistic transport at circuit level through simulation of several circuit demonstrators. The implementation of compact models in Verilog-A (SmartSpice [1]) environment offers the opportunity to describe as accurately as possible the physics of transport and to analyze its impact on various circuit elements.

Several analytical models based on the drift–diffusion formalism demonstrate that it is possible to introduce the diffusive transport in compact modelling. However, when the channel length approaches the value of mean free path, the mobility definition can no more strictly explain the electronic transport in the device [2]. In this case, we use the flux theory and the main parameter of this approach is the backscattering coefficient, which expresses the ballistic and the quasi-ballistic transport. Some well-known works performed by Lundstrom et al. [3–5] demonstrate the usefulness of the flux theory in qualitatively describing quasi-ballistic transport in compact modelling.

More recently, several works [6–8] proposed some accurate solutions to describe transport for nanoscale DG MOSFETs including quantum confinement or the effect of tunnelling through the source–drain potential barrier on devices characteristic. But few works [9,10] exposed the influence of ballistic/quasi-ballistic transport on the operation of the circuit demonstrator.

In this work, we demonstrate the feasibility of a simulation study of ballistic/quasi-ballistic transport at circuit level and we show the impact of this advanced transport on the switch of CMOS inverter and the oscillation frequency of ring oscillator. This paper is organised as follows: Section 2 explains the model physics and the corresponding assumptions. In Section 3, we explain our device simulation in ballistic and quasi-ballistic cases. Section 4 highlights the qualitative connection between physics of quasi-ballistic transport and its impact on circuit performance. Finally, we compare our model with numerical simulation in terms of CMOS switch and oscillation frequency.

2. DG MOSFET model

2.1 Ballistic and quasi-ballistic transport

The proposed analytical model (implemented in Verilog-A environment) is based on the well-known work of Natori [11] and Lundstrom and Ren [3]. This formula describes
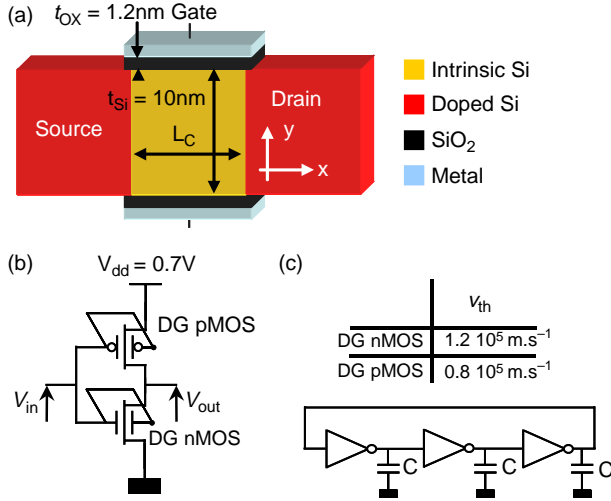
Figure 1.   DGMOS, (a) CMOS inverter, (b) ring oscillator and (c) definition of the main geometrical and electrical parameters.

the ballistic and quasi-ballistic current

$$I_D = W C_{ox}(V_{GS} - V_T)v_{th}\left(\frac{1-R}{1+R}\right)$$
$$\times \left(\frac{1 - e^{-qV_{DS}/kT}}{1 + [(1-R)/(1+R)]e^{-qV_{DS}/kT}}\right), \quad (1)$$

where W is the gate width; C_{ox} is the gate oxide capacitance; V_{GS} is the gate to source voltage; V_{DS} is the drain to source voltage; V_T is the threshold voltage; k is the Boltzmann constant; q is the electron charge and T is the lattice temperature.

In addition, Lundstrom et al. [4] developed physical compact models describing the device operation in quasi-ballistic regimes using the backscattering coefficient R [4]

$$R = \frac{L_{kT}}{L_{kT} + \lambda}; \quad L_{kT} = L_c \frac{kT}{qV_{DS}}, \quad (2)$$

where λ is the mean free path and L_{kT} is the distance over which the channel potential drops by kT/q compared with the peak value of the source to channel barrier. Physically, L_{kT} represents the critical distance over which scattering events modify the current; the limit and the demonstration of the backscattering coefficient are exposed [12].

We consider here the dynamical mean free path which is a 'local free path of ballistic carriers' [8]. This characteristic length represents the average distance to be crossed before the next scattering event. This approach considers that each carrier is ballistic as long as any event does not disturb its trajectory. The dynamic mean free path (dfp) connects the ballistic velocity and all interactions (coulomb and acoustic/optical phonon interaction) experienced by carriers crossing the channel. The scattering

process with impurities (τ_{imp}) and phonon interactions (τ_{ph}) are calculated as in [8] and the value of dfp used here is 27 nm in the intrinsic silicon channel. In practice, dfp replaces λ to describe quasi-ballistic transport

$$\mathrm{dfp} = v_{bal}\tau_{tot}; \begin{cases} \tau_{tot}^{-1} = \tau_{imp}^{-1} + \tau_{ph}^{-1}, \\ v_{bal} = \sqrt{\frac{2\varepsilon_{bal}}{m^*}}, \\ \varepsilon_{bal} = \frac{3}{2}kT + qV_{DS}, \end{cases} \quad (3)$$

where $m*$ is the mass in direction of transport; v_{bal} the ballistic velocity; τ_{tot} the total scattering rate and ε_{bal} the carrier energy.

2.2   Short channel effects

To obtain an accurate model and describe all electrostatic effects, we have also introduced short-channel effect and drain-induced barrier lowering (SCE/DIBL) using the Suzuki's model [13] for V_T. The starting point of this model is the Poisson equation, where the depleted and the electron charges are neglected

$$\frac{d^2\psi(x,y)}{dx^2} + \frac{d^2\psi(x,y)}{dy^2} = \frac{qN_A}{\varepsilon_{Si}} \approx 0. \quad (4)$$

Supposing a parabolic dependence in the y-direction

$$\frac{d^2\eta(x)}{d^2x} - \frac{\eta(x)}{\lambda^2} = 0, \quad (5a)$$

$$\lambda = \sqrt{\frac{\varepsilon_{Si}t_{Si}t_{ox}}{\varepsilon_{ox}}}, \quad (5b)$$

where $\eta = \psi_s(x) - V_{GS}$, $\psi_s(x)$ is the surface potential, ε_{Si} and ε_{ox} are, respectively, the silicon and the oxide permittivity. The solution of Equation (5a) is

$$\eta(x) = \frac{\eta_S \mathrm{sh}[(L_c - x)/\lambda] + \eta_S \mathrm{sh}(x/\lambda)}{\mathrm{sh}(L_c/\lambda)}, \quad (6)$$

where the boundary conditions are $\eta_S = \psi_S(0) - V_{GS}$ at the source and $\eta_D = \psi_S(L_c) - V_{GS}$ at the drain. $\psi_S(0)$ is the built-in potential equal to $(kT/q)\ln(N_D N_A/ni^2)$, N_D and N_A are, respectively, the doping level in the source/drain regions and in the channel.

The expression of the threshold voltage shift (ΔV_T) due to SCE/DIBL depends on the value of the minimum potential, given by

$$\psi_{S\,min}(x_{min}) = V_{GS} + 2\sqrt{\eta_S \eta_D}e^{L_c/4\lambda}, \quad (7)$$

$$x_{min} = \frac{L_c}{2} - \frac{\lambda}{2}\ln\left(\frac{\eta_D}{\eta_S}\right). \quad (8)$$

ΔV_T is then obtained from the following equation [13]:

$$\Delta V_T = 2\sqrt{\eta_S\,\eta_D}\,e^{-L_c/4\lambda}. \tag{9}$$

After some algebraic manipulation, we find the analytical expression of ΔV_T. Thus, V_T in Equation (1) is modified by ΔV_T, as follows:

$$V_T = V_{th} - \Delta V_T, \tag{10}$$

where V_{th} and ΔV_T are the long channel threshold voltage and its variation due to SCE/DIBL, respectively.

Finally, the above-threshold regime is linked to the subthreshold regime using an interpolation function based on the subthreshold swing S parameter, also defined by Suzuki et al. [13]

$$S = \frac{kT}{q}\ln(10)\left(\frac{\mathrm{d}\psi_{S\min}(x_{\min})}{\mathrm{d}V_{GS}}\right)^{-1}. \tag{11}$$

This assures the perfect continuity of our model between on-state regime and off-state regime.

3. Simulation results

3.1 Device simulations

After implementation in Verilog-A environment, the model has been used to simulate the DGMOS structure schematically presented in Figure 1. The source and drain regions are heavily doped $(1 \times 10^{20}\,\mathrm{cm}^{-3})$ and an intrinsic thin silicon channel is considered. The channel length varies from 10 to 200 nm; a gate oxide of 1.2 nm thick and a midgap metal gate are also considered.

It is well-known that the ballistic current is independent of channel length [11] except when SCE or DIBL appears. In order to clearly confirm this point, simulations have been performed for several length (20, 25, 30, 40, 50, 100 and 200 nm) and considering two types of transport (quasi-ballistic and ballistic; Figure 2). Note that for the ballistic case, the mean free path value has been chosen to be extremely large compared to the channel length. By contrast, to the ballistic case, the quasi-ballistic transport has the same behaviour as that of diffusive transport and the form of the output characteristics depends on L_c.

Figure 3 shows the drain current versus the gate voltage characteristics for the DGnMOS and DGpMOS simulated devices at $V_{DS} = 0.7\,\mathrm{V}$. In this approach, we suppose that the transport description (for ballistic and quasi-ballistic case) for holes is identical to that of electrons, with uniquely changing the thermal velocity value in non-degenerate conditions (Figure 1(b),(c), [14]). As expected, the ballistic and quasi-ballistic current shows a perfect continuity between the above and the subthreshold regime (as illustrated in Figure 3(a)). Finally,
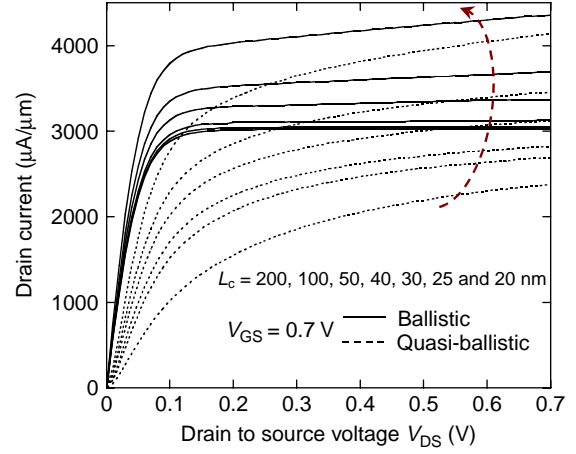

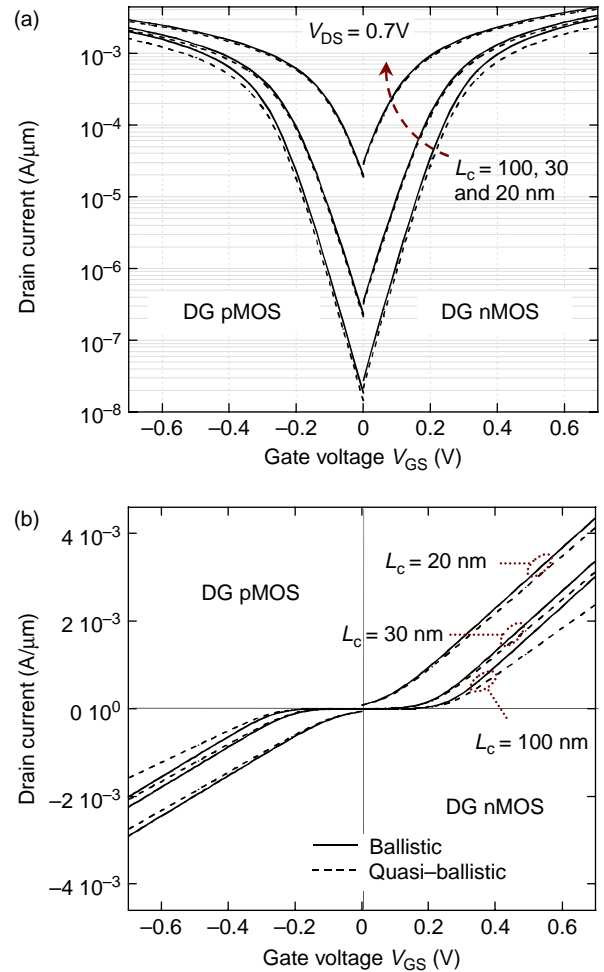Figure 2. Drain current versus V_{DS} for $L_c = 200$, 100, 50, 40, 30, 25 and 20 nm and $V_{GS} = 0.7\,\mathrm{V}$.

Figure 3. Drain current [(a) log and (b) lin scale] versus V_{GS} for $L_c = 100$, 30 and 20 nm. Solid line for ballistic transport and dashed line for quasi-ballistic transport.
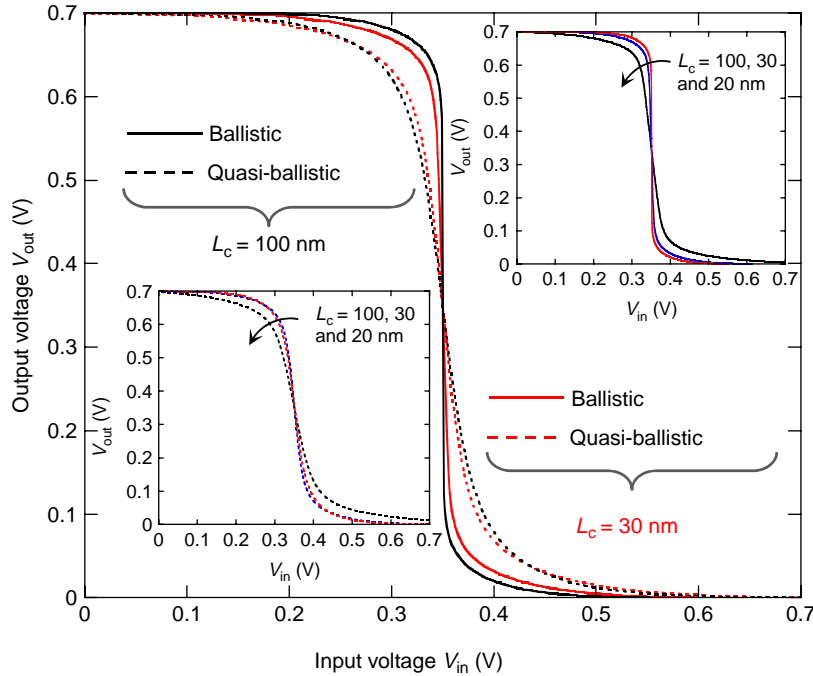
Figure 4. V_{out} versus V_{in} in a CMOS inverter. [Inset (a) and (b): transfer curve in ballistic and quasi-ballistic case for $L_c = 100$, 30 and 20 nm.]

Figure 3(b) shows that the DGnMOS and DGpMOS have the same behaviour in terms of transport, with different current levels due to the different values of thermal velocity.

3.2   Circuit simulations

In addition to the simulation of single device operation, we have simulated different circuit elements such as CMOS inverters and ring oscillators (Figure 1(b),(c)) to show the impact of ballistic/quasi-ballistic transport at circuit level.

The output voltage (V_{out}) of the CMOS inverter switches more sharply from the '1' state to the '0' state in the ballistic case than in quasi-ballistic transport (Figure 4). The switch of the CMOS inverter depends on the limit between linear and saturation region, which controls the switch between transistors. When SCE/DIBL occurs, the transition between linear and saturate regime is modified, and the switch from the '1' state to the '0' state is less sharp. In the quasi-ballistic case, the abruptness of the CMOS characteristic is strongly deteriorated. In conclusion, these results prove that the ballistic transport improves the switch and the static performances of the CMOS inverter.

Figure 5 shows the oscillation frequency as a function of the charge capacitance for two channel lengths: 100 and 30 nm. As expected, the oscillation frequency is reduced when the charge capacitance increases, due to variation of the propagation time through the inverters. We can also note the strong influence of short channel effects that increase the current value and reduce the difference between the oscillation frequencies in quasi-ballistic transport compared with ballistic transport.

Moreover, we thoroughly studied the influence of parasitic elements and phenomena on circuit performances. Figure 6(a) illustrates the impact of two charge capacitances on the oscillation frequency versus the
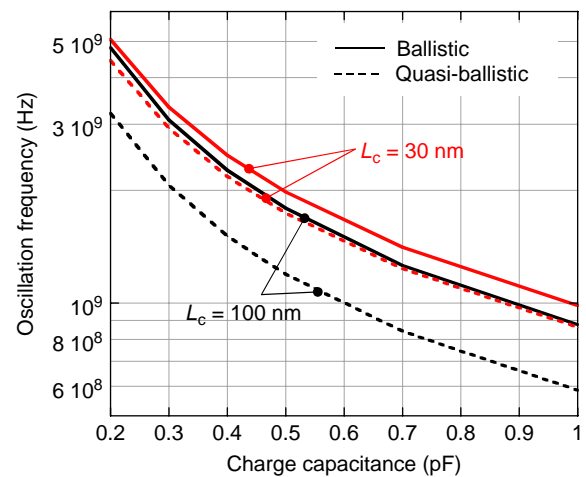

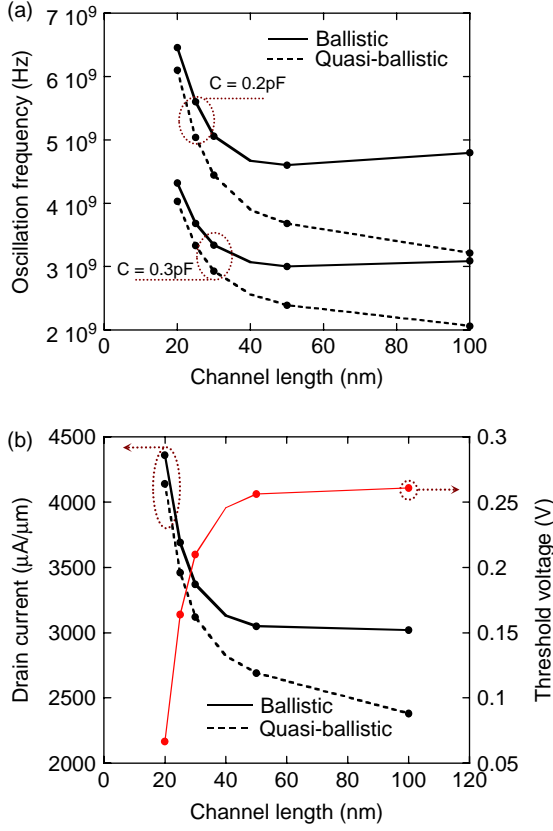Figure 5.   Oscillation frequency versus the charge capacitance for $L_c = 100$ and 30 nm.

Figure 6. (a) Oscillation frequency versus the channel length for $C = 0.2$ and $0.3\,\text{pF}$. (b) Drain current at $V_{DS} = V_{GS} = 0.7\,\text{V}$ and threshold voltage versus the channel.

channel length. Figure 6(b) shows the I_{on} current and V_T versus the channel length. This last figure demonstrates the strong influence of SCE/DIBL effect on the transient performance. The explanation is that when SCE/DIBL effects occur

- Firstly, the benefit of ballistic transport (versus quasi-ballistic) on the switch of the CMOS inverters is hidden (insets (a) and (b) of Figure 4).
- Secondly, the I_{on} current strongly increased (Figure 6(b)).

Consequently, the oscillation frequency in ballistic and quasi-ballistic case is less influenced by the value of the dfp.

These results show that the oscillation frequency is directly influenced by the type of transport (ballistic versus quasi-ballistic) that changes strongly the static and the transient performances. However, parasitic phenomena such as interconnect capacitances or SCE/DIBL are essential parameters in the analysis of circuit performances even when the intrinsic behaviour of transistors is dominated by ballistic transport.

4. Comparison with numerical simulation

4.1 Numerical simulation of ballistic transport using the quasi-ballistic mobility concept

In a previous work, we enhanced the pioneering approach of quasi-ballistic mobility proposed by Rhew and Lundstrom [15] and we introduced it into TCAD simulator, in order to numerically simulate the ballistic/quasi-ballistic transport using a TCAD tool. This approach, extensively presented in [9], is used here to validate our analytical model. In the following, we shortly remind the basic equations of this approach, based on the flux theory or McKelvey's flux method [2,15].

Figure 7 shows the schematics of the flux evolution in the channel (in the direction of transport). The two flux densities, F_D and F_S, incident on a semiconductor slab with thickness dx, transmit or reflect with the corresponding backscattering probabilities per length r [15]

$$\frac{dF_D(x)}{dx} = \underset{\rightarrow}{r}F_D(x) - \underset{\leftarrow}{r}F_S(x), \tag{12}$$

$$\frac{dF_S(x)}{dx} = \underset{\rightarrow}{r}F_D(x) - \underset{\leftarrow}{r}F_S(x), \tag{13}$$

where r is the scattering probabilities in the presence of an electric field and the symbols ' $\rightarrow$ ' and ' $\leftarrow$ ' of scattering probabilities represent the carrier's velocity components that are parallel or anti-parallel, respectively, to the electric field direction. Adding Equations (12) and (13) and considering $F = F_D - F_S$ and $n = (F_D + F_S)/v_{th}$ (where v_{th} is the thermal velocity) we obtain

$$\frac{dF}{dx} = \frac{d(F_D - F_S)}{dx} = 0, \tag{14}$$

$$F = \left(\frac{\underset{\leftarrow}{r} - \underset{\rightarrow}{r}}{\underset{\rightarrow}{r} + \underset{\leftarrow}{r}}\right) v_{th}n + \frac{v_{th}}{\underset{\rightarrow}{r} + \underset{\leftarrow}{r}}\frac{dn}{dx}. \tag{15}$$

We use here the expression of scattering probabilities proposed in [15] (with the assumption of non-degenerate gas) for the negative charge carrier

$$\underset{\leftarrow}{r} = \text{mfp}^{-1}; \quad \underset{\rightarrow}{r} = \text{mfp}^{-1} - \frac{qE(x)}{kT}, \tag{16}$$

where k is the Boltzmann constant; T is the lattice temperature; q is the electron charge; mfp is the mean free
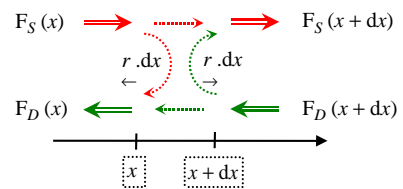

Figure 7. Description of the flux method parameters.

path and E is the electric field in the direction of transport. By analogy to the classical drift–diffusion approach, we obtain the Einstein relation; we define then a new mobility-like parameter, μ_{qb}, called quasi-ballistic mobility [7]

$$\mu_{qb} = \frac{v_{th}}{2(1/\text{mfp})(kT/q) + |E(x)|}. \qquad (17)$$

This quasi-ballistic mobility is introduced in TCAD software [9] (ATLAS SILVACO [16]). This approach represents an enhanced drift–diffusion-like approach to include quasi-ballistic and ballistic effects in the TCAD simulator. The quasi-ballistic mobility model is implemented using an explicit C-interpreter function describing the relation between the mobility and the parallel electric field (Equation (17)). All other quantities (such as the electrostatic potential, electric field, carrier concentration, current densities . . . /) are computed as usual in TCAD simulation, by solving the Poisson equation coupled to drift–diffusion transport equation. The details and the validation of this approach are explained in [9] and illustrated with simulations of small circuits based on DGMOS technology.

4.2   Comparison between numerical and analytical simulations

In order to validate the analytical model, we have compared our results with numerical simulation. Figure 8 compares the switch of the CMOS inverter in ballistic case for different channel lengths and illustrates the difference between our analytical model and numerical simulation.
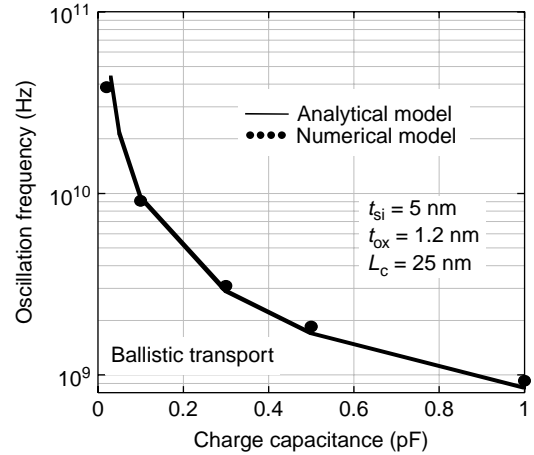
Figure 9.   Oscillation frequency versus charge capacitance for $t_{Si} = 5$ nm, $t_{ox} = 1.2$ nm, $L_c = 25$ nm. Comparison between our analytical model (solid line) and numerical simulation [9] (circle).

For the long channel case ($L_c = 100$ nm), the ballistic switch for numerical and analytical simulation perfectly matches. But for short channel ($L_c = 20$ nm) a small error is found in the comparison with numerical data. This is due to the fact that for $L_c = 20$ nm we approach the validity limit of our analytical model (which is $L_c = 2t_{Si}$ in the description of ΔV_T). Finally, the numerical simulations confirm the previous remark (exposed in paragraph 3) that short channel effects deteriorate the switch of the CMOS inverter.

Figure 9 compares the analytical and numerical oscillation frequency (for $t_{Si} = 5$ nm, $t_{ox} = 1.2$ nm, $L_c = 25$ nm) in the ballistic case for different charge capacitances. We note that an identical behaviour is obtained for the numerical and analytical data, which confirms the result of paragraph 3. Although, a small error exists (error attributed to the I_{on} value that is not exactly the same in analytical and numerical case), our analytical model shows a good agreement with the numerical simulation.

5.   Conclusion

In this work, a compact model for DGMOS taking into account ballistic and quasi-ballistic transport has been proposed and implemented in Verilog-A environment. Short channel effects and an interpolation function to link the above and the subthreshold voltage have been included to obtain a complete description of current characteristics. The dynamical mean free path definition was used to describe scattering processes with impurities and phonons. Finally, the model has been used to simulate two different small-circuits (CMOS inverter and ring oscillators) and to show the significant impact of ballistic/quasi-ballistic transport on the switch of CMOS inverter and the oscillation frequency of ring oscillator. Our simulation results prove that the ballistic transport improves the
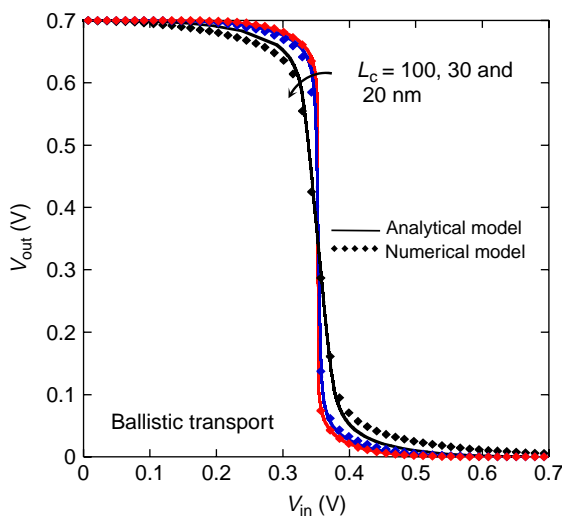
Figure 8. V_{out} versus V_{in} in a CMOS inverter for $t_{Si} = 5$ nm and $t_{ox} = 1.2$ nm. Comparison between numerical simulation (diamond) and our analytical model (solid line).

switch and the static performances of the CMOS inverter, and increases the oscillation frequency of ring oscillators. Finally, we have compared this model with numerical simulation in ballistic case; this comparison also validates our conclusions on the influence of short channel effects and ballistic transport on the operation of circuit elements.

This work also demonstrates the feasibility of a simulation study of ballistic/quasi-ballistic transport at circuit level and highlights the direct relation between the type of transport and static or transient performances of small-circuits.

Acknowledgements

References

[1] *SmartSpice Users' Manual*, (2008), Silvaco international, USA.
[2] J.P. McKelvey and J.C. Balogh, *Flux method for the analysis of transport problems in semiconductors in the presence of electric fields*, Phys. Rev. 137(A5) (1965), pp. A1555–A1561.
[3] M. Lundstrom and Z. Ren, *Essential physics of carrier transport in nanoscale MOSFETs*, IEEE Trans. Electron Dev. 49(1) (2002), pp. 131–141.
[4] M. Lundstrom, *Elementary scattering theory of the Si MOSFET*, IEEE Trans. Electron Dev. Lett. 18(7) (1997), pp. 361–363.
[5] A. Rahman and M.S. Lundstrom, *A compact scattering model for the nanoscale double gate MOSFET*, IEEE Trans. Electron Dev. 49(3) (2002), pp. 481–489.
[6] J.L. Autran, D. Munteanu, O. Tintori, E. Decarre, and A.M. Ionescu, *An analytical subthreshold current model for ballistic quantum-wire double gate MOS transistors*, Mol. Simul. 31(2/3) (2005), pp. 179–183.
[7] D. Munteanu, J.L. Autran, S. Harrison, K. Nehari, O. Tintori, and T. Skotniki, *Compact model of the quantum short-channel threshold voltage in symmetric double-gate MOSFET*, Mol. Simul. 31(12) (2005), pp. 831–837.
[8] E. Fuchs, P. Dollfus, S. Barraud, D. Villanueva, F. Salvetti, and T. Skotniki, *A new bascattering model giving a description of the quasi-ballistic transport in nano-MOSFET*, IEEE Trans. Electron Dev. 52(10) (2005), pp. 2280–2289.
[9] S. Martinie, G. Le Carval, D. Munteanu, and J.L. Autran, *Impact of ballistic transport on performances of double-gate MOSFETs-based circuits*, IEEE Trans. Electron Dev. 55(9) (2008), pp. 2443–2453.
[10] S. Martinie, D. Munteanu, G. Le Carval, and J.L. Autran, *A simple compact model to analyze the impact of ballistic and quasi-ballistic transport on ring oscillator performance*, in *Proceedings of the Integrated Circuit Design and Technology Conference (IcIcDt)*, Grenoble, France, June, 2008, pp. 273–276.
[11] K. Natori, *Ballistic metal-oxide-semiconductor field effect transistor*, J. Appl. Phys. 76(8) (1994), pp. 4879–4890.
[12] S. Martinie, D. Munteanu, G. Le Carval, and J.L. Autran, *New unified analytical model of backscattering coefficient from low to high field conditions in quasi-ballistic transport*, IEEE Electron Dev. Lett. 29(12) (2008), pp. 1392–1394.
[13] K. Suzuki, Y. Tosaka, and T. Sugii, *Analytical threshold voltage for short channel n + −p + double-gate SOI MOSFETs*, IEEE Trans. Electron Dev. 43(5) (1996), pp. 732–738.
[14] F. Assad, Z. Ren, S. Datta, M. Lundstrom, and P. Bendix, *Performance limits of silicon MOSFET's*, IEEE IEDM Tech. Dig. (1999), pp. 547–550.
[15] J-H. Rhew and M.S. Lundstrom, *Drift–diffusion equation for ballistic transport in nanoscale metal-oxide-semiconductor field effects transistor*, J. Appl. Phys. 92(9) (2002), pp. 5196–5202.
[16] *Silvaco-ATLAS Users' Manual*, Silvaco international, USA.